

ABSTRACT

-- A method for synthesizing a register transfer level (RTL) based design employs a bottom-up approach to generate a final top-level design. The top-level design is divided into a plurality of sub-modules. Each of the sub-modules is then independently synthesized using an RTL based design approach and independently adapted to conform to timing requirements produced for each of the sub-modules using time budgets that are based on the top-level timing requirements. Once the sub-modules are synthesized and pass individual timing requirements specific for those sub-modules, the sub-modules are integrated to form a top-level design. The top-level design may then be verified for timing requirements and other formal requirements.--